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	US 5319229 A		US 5780893 A		US 6144062 A	US 5619051 A		US 5753952 A		US 6130452 A		US 6172394 B1		US 6054731 A	US 6188101 B1	Document ID
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	18		13		35	<u> </u>		H H	,	16		16		9	<i>ა</i>	Pages
retention time	Semiconductor nonvolatile memory with wide memory window and long data	with a composite gate structure	Non-volatile semiconductor memory device including memory transistor	and_method_of_manufacture	Semiconductor device having thin electrode layer adjacent gate insulator	Semiconductor nonvolatile memory cell	gate		and method of fabrication	Virtual ground flash cell with asymmetrically placed source and drain	protruding conductive	Non-volatile semiconductor memory device having a floating gate with	manufacturing_method	Floating gate non-volatile memory cell with low erasing voltage and	Flash EPROM cell with reduced short channel effect and method for providing	Title
	257/324		257/318		257/317	257/316		257/316		257/315		257/315		257/314	257/314	Current OR
; 438/287	257/406 ; 257/411 ; 257/637 ; 257/640 : 257/645	; 257/316 ; 257/317 ; 257/322	257/262 ; 257/264 ; 257/314 ; 257/315		257/315 ; 257/321	257/324 ; 257/325 ; 257/411	; 365/185.1 ; 438/264	257/315 ; 257/317 ; 257/318 ; 365/185.01		257/321	; 438/304	257/288 ; 257/387 ; 438/257		257/316 ; 257/324	257/315 ; 257/404 ; 257/640 ; 257/914	Current XRef
	Shimoji, Noriyuki , et al.		Sugaya, Fumitaka		Mine, Toshiyuki , et al.	Endo, Nobuhiro		Mehrad, Freidoon		Lu, Wenpin , et al.		Nakagawa, Shinichi		Cappelletti, Paolo	Wang, Janet	Inventor

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	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
10	US 6236085 B1	20010522	N 5	Semiconductor memory device having high-concentration region around electric-field moderating layer in substrate	257/345	257/315 ; 257/316 ; 257/318 ; 257/320 ; 257/321 ; 257/322 ; 257/322 ; 257/336 ; 257/344 ; 257/408 ; 257/408 ; 257/900	Kawaguchi, Tsutomu , et al.
11	US 6137718 A	20001024	σ	Method for operating a non-volatile memory cell arrangement	365/185.03	257/324 ; 365/185.28	Reisinger, Hans
12	US 4996571 A	19910226	15	tor memory	365/185.19	257/321 ; 365/185.06 ; 365/185.09 ; 365/185.23 ; 365/185.3 ; 365/218	Kume, Hitoshi , et al.
13	US 5432749 A	19950711	7	Non-volatile memory cell having hole confinement layer for reducing	365/218	257/315 ; 365/185.17	Sethi, Rakesh B.
14	US 5904518 A	19990518	18	Method of manufacturing a semiconductor IC device having single transistor type nonvolatile	438/201	438/258	Komori, Kazuhiro , et al.
15	US 6238967 B1	20010529	14	memory cells Method of forming embedded DRAM structure	438/244	438/243	Shiho, Yasuhito , et al.
16	US 5814543 A	19980929	35	Method of manufacturing a semicondutor integrated circuit device having	438/264	438/265 ; 438/592	Nishimoto, Toshiaki , et al.
				nonvolatile memory cells			

	Туре	Hits	Search Text	DBs	Time Stamp
1	IS&R	10	(("4577215") or ("5482879") or ("5879992") or ("6229176") or ("5016068") or ("5295107") or ("6046086") or ("4442447") or ("4513397") or ("4592130")).PN.	USPAT: US-PGPUB	2001/09/17 08:33
2	IS&R	40	(("4618876") or ("4903097") or ("5526307") or ("5760435") or ("6069381") or ("6207989") or ("6239465") or ("4417264") or ("4588339") or ("4590665") or ("4802137") or ("5212541") or ("5216268") or ("5289026") or ("5289026") or ("5289026") or ("5447877") or ("5457061") or ("547877") or ("5605853") or ("5612237") or ("5625213") or ("5702965") or ("5811880") or ("5852312") or ("58588840") or ("5877525") or ("5940705") or ("5946240") or ("5950087") or ("5972753") or ("6034892") or ("6124168") or ("6180977") or ("6188102")).PN.	USPAT: US-PGPUB	2001/09/17 08:33
3	IS&R	54	("438/288").CCLS.	USPAT; US-PGPUB	2001/09/17 09:30
4	IS&R	652	("257/315").CCLS.	USPAT: US-PGPUB	2001/09/17 09:56
5	IS&R	309	("257/324").CCLS.	USPAT; US-PGPUB	2001/09/17 09:56
6	BRS	267	(("257/324").CCLS.) not (("257/315").CCLS.)	USPAT; US-PGPUB	2001/09/17 09:57
7	BRS	342	asymmetric same source same drain	USPAT: US-PGPUB	2001/09/17 11:13
8	BRS	240	asymmetric with source with drain	USPAT: US-PGPUB	2001/09/17 11:13
9	BRS	159	(asymmetric with source with drain) and memory	USPAT; US-PGPUB	2001/09/17 11:14